Redesign Procedure for Two-Stage CMOS Op amp with Least Error of Frequency Response and Phase Margin

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***Abstract*—This paper presents a redesign procedure for two-stage CMOS op amp with least error of frequency response and phase margin. Design procedure for two-stage op amp is followed by the proposed in [8]. To prove the performance of the proposed redesign procedure steps, Cadence simulation results are given. The proposed redesign procedure for two-stage CMOS op amp is implemented in AMS 0.35 µm CMOS technology. The simulation results show in ±2.5 V power supply, frequency response is 5.7 MHz with -5.83% error, phase margin is 60.36 with 0.6 % error. Compare with previous work, our design procedure has least error of frequency response and phase margin.**

Keywords—Design procedure; two-stage op amp; phase margin.

I. INTRODUCTION

Operational Amplifiers (op amps) are widely employed in analog signal processing and data conversion such as successive approximation register (SAR) and digital-to-analog converter (DAC) [1]-[4]. Moreover, it can be used in RF systems for wireless communications [5]-[6]. Operational Amplifiers (op amps) are vital part in analog signal processing and data conversion circuits. One of the most popular CMOS op amp structure is the two-stage op amp structure shown in Fig. 1. The designing of an op amp is complicated as it involves a number of specifications such as gain, bandwidth, common-mode range, offset, signal swing and slew rate. Design procedure of the two-stage op amp with Miller capacitor and resistor compensation are presented in [7]. The improved design procedure of this type of op amp which allows greater degree of freedom in performance trade-off was proposed in [8].

However, it will be shown that one of the drawbacks of the procedure in [8] is that the unity-gain frequency is assumed to be the same as gain-bandwidth. This causes some characteristics of the designed op amp, notably unity-gain frequency and phase margin, to be deviate from the specifications and some tweaks of design parameters are necessary.

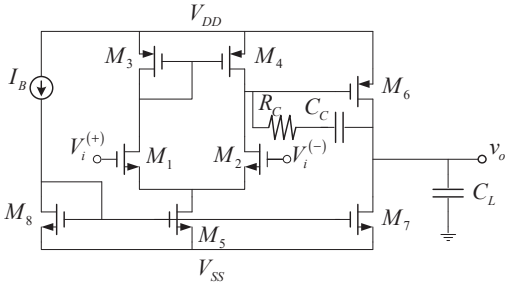


Fig. 1. Two-stage CMOS op amp

In this work the design procedure in [8] will be modified such that the unity-gain frequency and phase margin of the designed op amps are much closer to the specifications.

II. MORE ACCURATE FORMULA FOR UNITY-GAIN FREQUENCY AND PHASE MARGIN

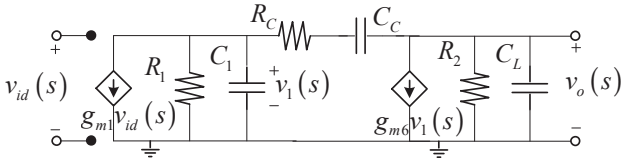


Fig. 2. Small-signal equivalent circuit of single-ended CMOS op amp in Fig.1 where $R_1 = r_{ds2}//r_{ds4}$ and $R_2 = r_{ds6}//r_{ds7}$.

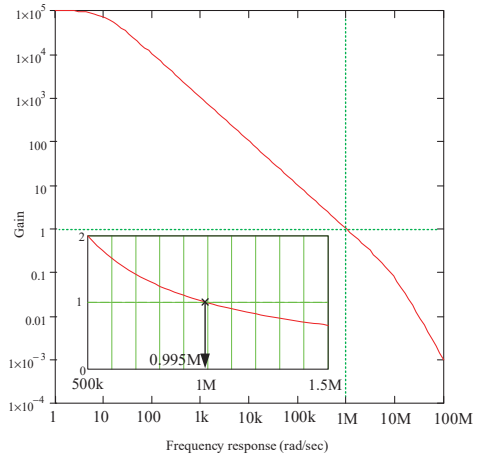
By analyzing the small-signal equivalent circuit in Fig. 2, the transfer function of the two-pole op amp in Fig. 1 is given by

$$H(s) = A_o \frac{1 - sC_c\left(1/g_{m6} - R_c\right)}{R_1R_2R_cC_{gs6}C_cC_Ls^3 + R_1R_2\left(C_{gs6}C_L + C_{gs6}C_c + C_cC_L\right)s^2 + g_{m6}R_1R_2C_cs + 1} \quad (1)$$

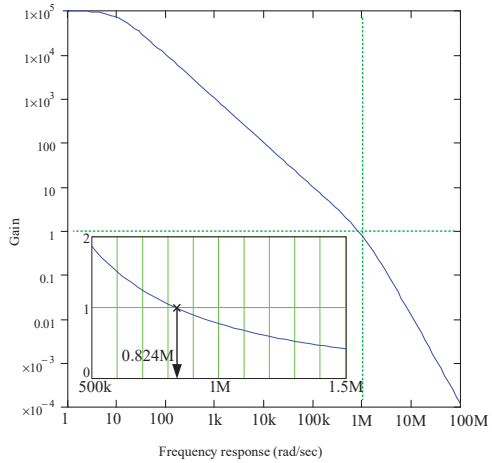
It can be observed that such a transfer function has three poles and one zero. Under certain condition, one of the poles and the zero can be made to cancel out, reducing the transfer function to have only two poles, i.e.

$$A(s) = \frac{A_o}{\left(1 + s/\omega_{dp}\right)\left(1 + s/\omega_{np}\right)} \quad (2)$$

where ω_{dp} = -p_{dp} and ω_{np} = -p_{np} are dominant pole frequency and non-dominant pole frequency, respectively. Although it is normally assumed that the unity-gain frequency ω_u can be accurately approximated by the gain-bandwidth product ω_{GBW} = $A_o\omega_{dp}$, this is not the case if the ω_{np} is not large enough as demonstrated in Fig. 3(a) and (b).



(a)ω_{np} is large enough (ω_{np} /ω_{GBW} =10)



(b) ω_{np} is not large enough (ω_{np} /ω_{GBW} =2)

Fig. 3. Frequency response of the transferfunction in (2).

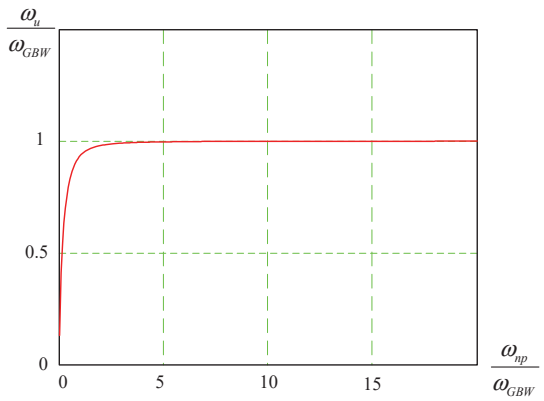


Fig. 4. The plot of ω_u/ω_{GBW} versus ω_{np}/ω_{GBW}

For, $\omega \gg \omega_{dp}$, equation (2) can be approximated as

$$A(s) \cong \frac{\omega_{GBW}}{s\left(1 + s/\omega_{np}\right)} \quad (3)$$

where

$$\omega_{GBW} = A_o\omega_{dp} \quad (4)$$

and thus

$$\left|A(j\omega_u)\right| \cong \frac{\omega_{GBW}}{\omega_u\left(1 + \frac{\omega_u^2}{\omega_{np}^2}\right)} = 1. \quad (5)$$

Rearranging the equation (5), yields

$$\frac{\omega_u^4}{\omega_{np}^2} + \omega_u^2 - \omega_{GBW}^2 = 0. \quad (6)$$

By solving the equation (6), it can be found to be

$$\omega_u = \frac{\omega_{np}}{b} \quad (7)$$

where

$$b = \sqrt{\frac{2}{\sqrt{1+4/a^2}-1}} \tag{8}$$

and

$$a = \frac{\omega_{np}}{\omega_{GBW}}. \tag{9}$$

Fig. 4 shows the plot of equation (7)-(9) where the influence of the non-dominant pole frequency over the unity-gain frequency can be clearly observed.

Phase margin of the op amp is given by [9]

$$\phi_M = \angle A(j\omega_u) - (-180°). \tag{10}$$

From equations (3) and (10), we found that

$$\angle A(j\omega_u) \cong \angle \frac{1}{j\left(1+j\omega_u/j\omega_{np}\right)} = -90° - \tan^{-1}\frac{\omega_u}{\omega_{np}}. \tag{11}$$

Substituting (11) into (10) and rearranging, we have

$$\phi_M = \tan^{-1}\frac{\omega_{np}}{\omega_u}. \tag{12}$$

Substituting (7) and (8) into (12) yields

$$\phi_M = \tan^{-1}\sqrt{\frac{2}{\sqrt{1+4/a^2}-1}}. \tag{13}$$

Substituting (7) - (9) into (13) yields

$$\omega_{GBW} = \frac{\omega_u \tan\phi_M}{2}\sqrt{\left(\frac{2}{\tan^2\phi_M}+1\right)^2-1}. \tag{14}$$

For, $g_{m1} = \sqrt{2\mu_n C_{ox}(W/L)_{1,2} I_{D1}}$, $I_{D1} = I_{D5}/2$, $\omega_{GBW} = g_{m1}/C_C$ and $I_{D5} = SR \times C_C$ are given by [8]

$$\left(\frac{W}{L}\right)_{1,2} = \frac{\omega_{GBW}^2 C_C}{SR\mu_n C_{ox}} \tag{15}$$

Substituting (14) into (15) yields

$$\left(\frac{W}{L}\right)_{1,2} = \frac{C_C\omega_u^2\tan^2\phi_M}{4SR\mu_n C_{ox}}\left[\left(\frac{2}{\tan^2\phi_M}+1\right)^2-1\right] \tag{16}$$

The design steps can be followed by [8], and it can be summarized as shown in Table I.

TABLE I. OP AMP DESIGN STEP

Step	[8]	This proposed
1	$C_C = \frac{16kT}{3\omega_u S_n(f)}\left[1+\frac{SR}{\omega_u\left(V_{HR}^{CM+}+V_{tn}\right)}\right]$	
2	$I_{D7} = SR(C_C + C_L)$	
3	$L_6 = \sqrt{\frac{3SR\mu_p V_{HR}^{Out+} C_c}{2\omega_u I_{D7}\tan(\phi_M)}}$	
4	$W_6 = \frac{2I_{D7}}{\mu_p C_{ox}\left(V_{HR}^{Out+}\right)^2}L_6$	
5	$I_{D5} = C_C SR$	
6	*	**
7	$(W/L)_{5,8} = \frac{2I_{D5}}{\mu_n C_{ox}\left(V_{HR}^{CM-}-V_{th}-SR/\omega_u\right)^2}$	
8	$(W/L)_7 = \left(\frac{C_c+C_L}{C_c}\right)(W/L)_{5,8}$	
9	$(W/L)_{3,4} = \frac{(W/L)_6}{2(W/L)_7}(W/L)_{5,8}$	

$$*\left(\frac{W}{L}\right)_{1,2} = \frac{\omega_u^2 C_C}{SR\mu_n C_{ox}}$$

$$**\left(\frac{W}{L}\right)_{1,2} = \frac{C_C\omega_u^2\tan^2\phi_M}{4SR\mu_n C_{ox}}\left[\left(\frac{2}{\tan^2\phi_M}+1\right)^2-1\right]$$

III. SIMULATION RESULTS

For the process parameters of AMS 0.35 µm CMOS technology shown in Table II and op amp specification shown in Table III, design parameters of op amp in Fig. 1 are obtained from our proposed redesign procedure, step 1 to step 9, and the design procedure proposed in [8].

TABLE II. PROCESS PARAMETERS

Parameters	NMOS	PMOS
$\mu(\mathrm{m/V\cdot S})$	25×10^{-3}	9.213×10^{-3}
$Tox(\mathrm{m})$	7.575×10^{-9}	7.575×10^{-9}
$V_t(\mathrm{V})$	0.4979	0.6842

TABLE III. DESIGN PARAMETERS

Ratio	[8]	This Work	Unit
$(W/L)_{1,2}$	1.904 / 1	2.539 / 1	µm/µm
$(W/L)_{3,4}$	1.458 / 1	1.458 / 1	µm/µm
$(W/L)_{5,8}$	38.1 / 1	38.1 / 1	µm/µm
$(W/L)_{6}$	41.64 / 4.759	41.64 / 4.759	µm/µm
$(W/L)_{7}$	1.143 / 1	1.143 / 1	µm/µm

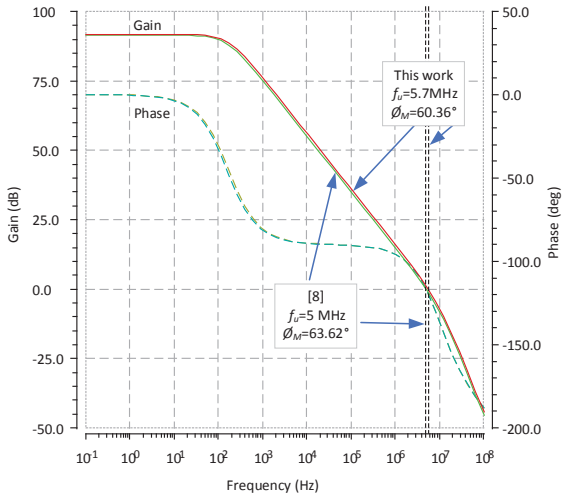


Fig. 5. Loop-gain frequency response of two-stage CMOS op amp.

Simulation result of loop-gain frequency response is shown in Fig.5. The results of the design procedure for two-stage CMOS op amp from [8], frequency response and phase margin are f_u = 5MHz ($f_{u\text{-}error}$ = -16.67%), $Ø_M$ = 63.62° ($Ø_{M\text{-}error}$ = 6.03%), respectively. The results of our redesign procedure, frequency response and phase margin are f_u = 5.7 MHz ($f_{u\text{-}error}$ = -5.83%), $Ø_M$ = 60.36° ($Ø_{M\text{-}error}$ = 0.6%), respectively. Table IV summarizes the simulation results, for R_C =28.32kΩ, C_C = 1pF, C_L=2pF, I_{D5}=6.464 µA and I_{D7} = 18.6 µA, of this work and compare it with [8]. The proposed redesign procedure for two-stage CMOS op amp achieve least error of frequency response and phase margin than in [8].

TABLE IV. SIMULATION RESULTS

Parameters	[8]	This Work
A_o(dB)	91.3	91.62
f_u (MHz)	5	5.7
$f_{u\text{-}error}$ (%)	-16.67	-5.83
$Ø_M$ (Deg)	63.62	60.36
$Ø_{M\text{-}error}$(%)	6.03	0.6

IV. CONCLUSION

The redesign procedure for two-stage CMOS op amp has been presented. Simulation results confirm that the proposed redesign step is least error of frequency response and phase margin than the one proposed in [8].

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