

Regular paper

New method to design feedback amplifier employing two-stage CMOS op amp

Chaiyan Chanapromma^{*}, Jirayuth Mahattanakul

The Electrical Engineering Graduate Program, Faculty of Engineering, Mahanakorn University of Technology Bangkok, Thailand



ARTICLE INFO

Keywords:

Amplifier
Two-stage
CMOS
Op amp
Current buffer

ABSTRACT

A new method to design feedback amplifier employing two-stage CMOS op amp is proposed. It is shown that although the open-loop phase margin of around 65 degrees is suitable for op amp connected as unity-gain amplifier (100% feedback), such is not the case when amplifier's feedback factor of is less than 100%. In the proposed design method, the open-loop phase margin requirement is replaced by closed-loop bandwidth and quality factor of feedback amplifier such that a better control of the responses of the amplifier is achieved. Comparison of simulation results of feedback amplifiers obtained from the traditional method and the proposed method is given. It is demonstrated that the inverting amplifier obtained from the proposed method consumes somewhat less power than the one obtained from the traditional design, which employs the op amp with 65 degrees phase margin, while having comparable gain, bandwidth, transient and noise performances.

1. Introduction

Although electronic feedback amplifier can be realized using many types of active elements, op amp is one of the most versatile building blocks in analog and mixed-signal systems and hence op amp based feedback amplifier is one of the most widely used types of feedback amplifier [1–11]. In op amp design, frequency compensation (Fig. 1) is employed to move poles and zeros in such a way that, when used in the negative feedback configuration, the circuit's frequency and transient responses are well controlled. It can be shown that if an op amp is modeled as a two-pole system, a phase margin close to 65 degrees would make the frequency response of the op amp with 100% feedback, i.e. connected as a unity-gain voltage buffer, to be maximally flat (quality factor $Q = 0.707$). Hence in traditional op amp design, the open-loop phase margin of certain value, normally around 60–70 degrees, is targeted, as exhibited in Table 1. Although it is convenient to fully compensate an op amp for all applications, this procedure is rather wasteful [24]. However, when designing op amps to be used as fixed-gain feedback amplifiers in specific integrated circuits, the phase margin requirement, which is suitable for 100% feedback, may lead to overcompensation for amplifiers with less than 100% feedback.

In this paper, a new method to design an op amp to be employed as a feedback amplifier is proposed. In the proposed method, open-loop phase margin requirement is replaced by closed-loop bandwidth and

quality factor (to ensure maximally flat response) of the feedback amplifier. Since the proposed method allows for the overcompensation to be avoided, power consumption of the feedback amplifier can be reduced significantly.

2. Phase margin requirement for maximally flat response

The transfer function of an op amp modeled by a system with one dominant pole p_1 and one non-dominant pole p_2 is given by

$$A(s) = \frac{A_o}{(1 + s/\omega_{dp})(1 + s/\omega_{np})} \quad (1)$$

where $\omega_{dp} = -p_1$, $\omega_{np} = -p_2$ and A_o are dominant pole frequency, non-dominant pole frequency and DC gain, respectively. For frequencies well above ω_{dp} , Eq. (1) can be approximated as

$$A(s) \cong \frac{\omega_{GBW}}{s(1 + s/\omega_{np})} \quad (2)$$

where

$$\omega_{GBW} = A_o\omega_{dp} \quad (3)$$

is the gain-bandwidth product of the op amp. By denoting ω_u as the unity-gain frequency, we have

^{*} Corresponding author.

E-mail addresses: tony_1182912@hotmail.com (C. Chanapromma), jirayut@mut.ac.th (J. Mahattanakul).

$$|A(j\omega_u)| \cong \frac{\omega_{GBW}}{\omega_u \left(1 + \frac{\omega_u^2}{\omega_{np}^2}\right)} = 1. \quad (4)$$

By re-arranging (4), we obtain the quadratic equation

$$\frac{\omega_u^4}{\omega_{np}^2} + \omega_u^2 - \omega_{GBW}^2 = 0 \quad (5)$$

in which ω_u can be found to be

$$\omega_u = \frac{\omega_{np}}{b} \quad (6)$$

where

$$b = \frac{\sqrt{2}}{\sqrt{\sqrt{1 + 4\left(\frac{\omega_{GBW}}{\omega_{np}}\right)^2} - 1}}. \quad (7)$$

Phase margin of the op amp is defined as

$$\phi_M = \angle A(j\omega_u) - (-180^\circ). \quad (8)$$

From Eq. (2), the phase response of the system is given by

$$\angle A(j\omega_u) = -90^\circ - \tan^{-1} \frac{\omega_u}{\omega_{np}}. \quad (9)$$

Substituting (8) into (9) yields

$$\phi_M = 90^\circ - \tan^{-1} \frac{\omega_u}{\omega_{np}} = \tan^{-1} \frac{\omega_{np}}{\omega_u}. \quad (10)$$

Subsequently, by substituting (6) into (10), we obtain

$$\phi_M = \tan^{-1} \frac{\sqrt{2}}{\sqrt{\sqrt{1 + 4\left(\frac{\omega_{GBW}}{\omega_{np}}\right)^2} - 1}}. \quad (11)$$

Referring to the circuit in Fig. 2(a), assuming that the op amp has infinite input resistance and zero output resistance, the transfer function of the circuit is given by

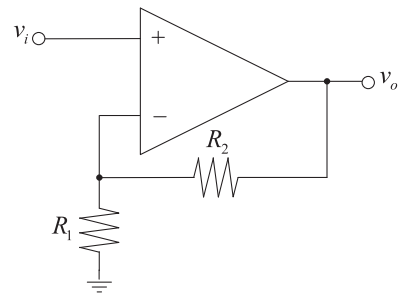
$$\frac{v_o(s)}{v_i(s)} = \frac{A(s)}{1 + A(s)B} \quad (12)$$

where $A(s)$ is the open-loop transfer function of the op amp and

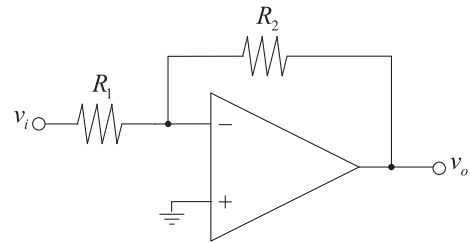
$$B = \frac{R_1}{R_1 + R_2} \quad (13)$$

Table 1
Phase margin requirement used or suggested in the literature.

| Reference | Phase Margin (ϕ_M) |
|-----------|---------------------------|
| [12] | 70° |
| [13] | 65° |
| [14] | 60° |
| [15] | 60° |
| [16] | 65° |
| [17] | 65° |
| [18] | 77° |
| [19] | 65° |
| [20] | 62.1° |
| [21] | 66.5° |
| [22] | 65.56° |
| [23] | 65° |



(a)



(b)

Fig. 2. (a) Non-inverting and (b) Inverting gain op-amp based amplifier.

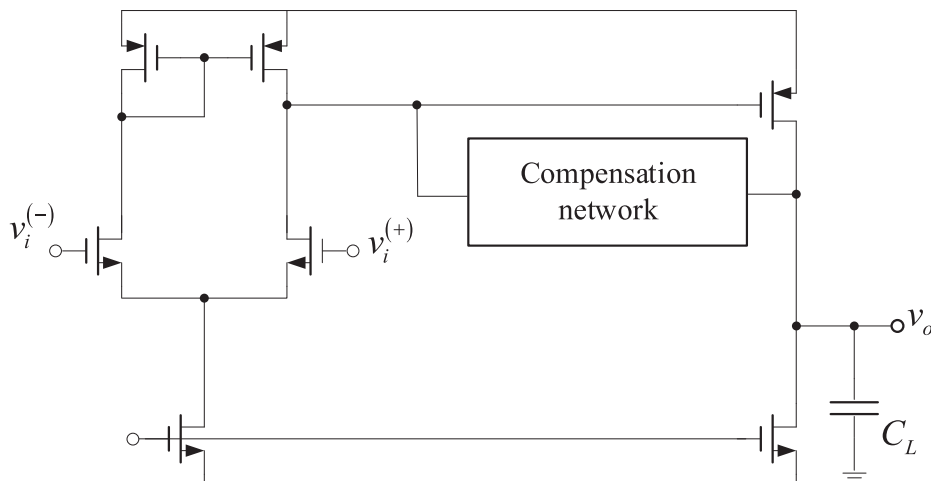


Fig. 1. Unbuffered two-stage CMOS op amp with compensation network connected across high-gain stage.

is the feedback factor of the circuit whose value ranges between 0 and 1. Substituting (1) into (12) and re-arranging the result yields

$$\frac{v_o(s)}{v_i(s)} = \frac{A_o \omega_{dp} \omega_{np}}{s^2 + s(\omega_{dp} + \omega_{np}) + (1 + A_o B) \omega_{dp} \omega_{np}} \quad (14)$$

Under the dominant pole condition $\omega_{np} \gg \omega_{dp}$ and high DC gain $A_o \gg 1/B$, Eq. (14) can be approximated as

$$\frac{v_o(s)}{v_i(s)} = \frac{A_o \omega_{dp} \omega_{np}}{s^2 + s\omega_{np} + B A_o \omega_{dp} \omega_{np}} \quad (15)$$

which when combined with (3) is equivalent to

$$\frac{v_o(s)}{v_i(s)} = \frac{\omega_{GBW} \omega_{np}}{s^2 + s\omega_{np} + B \omega_{GBW} \omega_{np}} \quad (16)$$

Substituting (13) into (16) and re-arranging the result, we re-express the transfer function of the non-inverting amplifier in Fig. 2(a) as

$$\frac{v_o(s)}{v_i(s)} = \left(1 + \frac{R_2}{R_1}\right) \times \left(\frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}\right) \quad (17)$$

where the first factor of the RHS of the equation is the ideal gain of the non-inverting amplifier and the second factor is the error function in which the natural frequency ω_o and the quality factor Q are given by

$$\omega_o = \sqrt{B \omega_{GBW} \omega_{np}} \quad (18)$$

and

$$Q = \sqrt{\frac{B \omega_{GBW}}{\omega_{np}}} \quad (19)$$

respectively.

Likewise by analyzing the circuit in Fig. 2(b), we obtain

$$\frac{v_o(s)}{v_i(s)} = \left(-\frac{R_2}{R_1}\right) \times \left(\frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}\right) \quad (20)$$

where the first factor of the RHS of the equation is the ideal gain of the inverting amplifier and the second factor is the error function in which the expression for the natural frequency ω_o and the quality factor Q are given by Eqs. (18) and (19) respectively. By comparing Eqs. (17)–(20), we found that the error functions of the circuits in Fig. 2(a) and (b) are the same and therefore apart from the DC gain, their frequency responses would be the same.

It should also be noted that the ideal DC gain of the non-inverting amplifier in Fig. 2(a) is $1/B$ while the ideal DC gain of the inverting

amplifier in Fig. 2(b) is $1 - 1/B$. For instance, for $B = 0.5$ (50% feedback), the ideal DC gain of the non-inverting amplifier in Fig. 2(a) is $1/0.5 = 2$ while the ideal DC gain of the inverting amplifier in Fig. 2(b) is $1 - 1/0.5 = -1$.

By combining (11) and (19) we obtain

$$\phi_M = \tan^{-1} \sqrt{\frac{2}{\sqrt{1 + \frac{4Q^4}{B^2}} - 1}} \quad (21)$$

For $Q = 1/\sqrt{2}$, i.e. maximally flat response, Eq. (21) becomes

$$\phi_M = \tan^{-1} \sqrt{\frac{2}{\sqrt{1 + \frac{1}{B^2}} - 1}} \quad (22)$$

According to Eq. (22), the plot of phase margin ϕ_M VS feedback factor B is illustrated in Fig. 3 where it can be observed that for $B = 1$ (100% feedback), the value of ϕ_M around 65 degrees is required for Q to be 0.707. However, for other values of B less than unity, the required value of ϕ_M which makes $Q = 0.707$ is lower than 65 degrees, e.g., for $B = 1/3$ (which corresponds to gain of 3 for non-inverting amp and gain of -2 for inverting amp), the value of ϕ_M of around 44 degrees is required.

3. Proposed op amp based feedback amplifier design

In this section the two-stage CMOS op amp in Fig. 4 will be used to illustrate the new method to design op amp to be used as a feedback amplifier. The small-signal equivalent circuit of the CMOS op amp in Fig. 4 is shown in Fig. 5 in which the first stage of the op amp is modeled by a voltage controlled current source as it is usually much faster than the second stage [13,24,25].

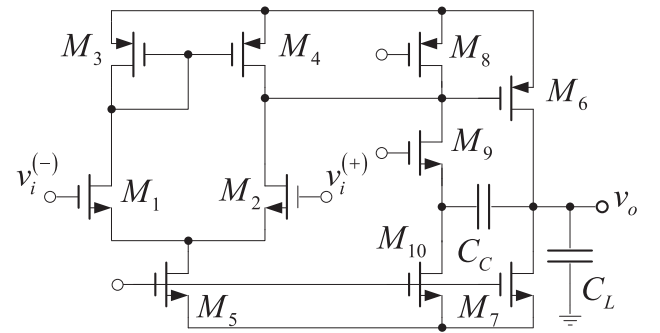


Fig. 4. Two-stage CMOS op amp with a Miller capacitor and a current buffer as compensation network.

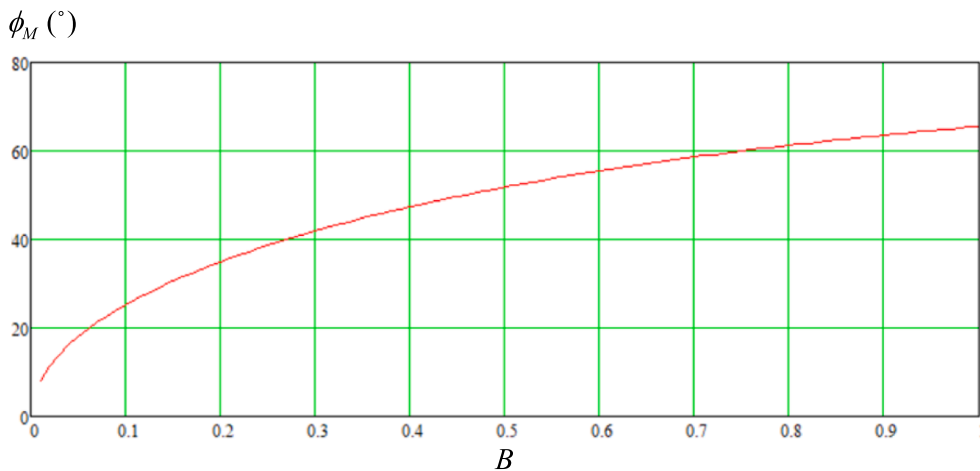


Fig. 3. Graph of ϕ_M VS B for $Q = 0.707$ (maximally flat response).

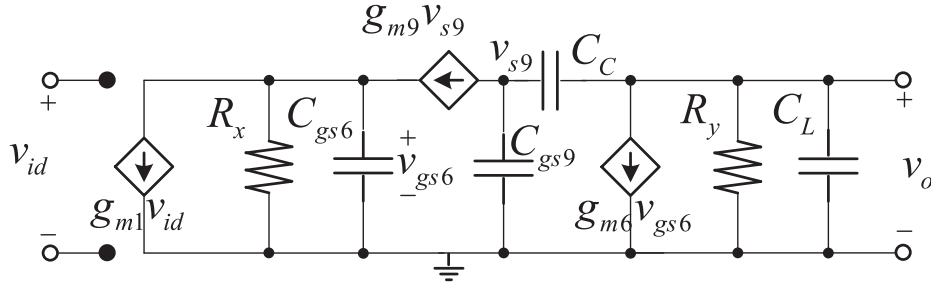


Fig. 5. Small-signal equivalent circuit of the CMOS op amp in Fig. 4, where $R_x = r_{ds2}/r_{ds4}$ and $R_y = r_{ds6}/r_{ds7}$.

By analyzing the circuit in Fig. 5, the open-loop transfer function of the op amp in Fig. 4 was found to be

$$A_{OL}(s) = \frac{v_o(s)}{v_{id}(s)} = \frac{g_{m1}g_{m6}R_xR_y}{1 + sg_{m6}R_xR_yC_C} \times \frac{1 + s\left(\frac{C_C + C_{gs9}}{g_{m9}}\right)}{s^2\left(\frac{C_L C_{gs6}}{C_C g_{m6}} \times \frac{C_C + C_{gs9}}{g_{m9}}\right) + s\left(\frac{C_L C_{gs6}}{C_C g_{m6}} \times \frac{C_{gs6}}{g_{m6}}\right) + 1} \quad (23)$$

which has three poles and one zero. By inspection, it can be found that under the design condition

$$\frac{g_{m9}}{C_C + C_{gs9}} = \frac{g_{m6}}{C_{gs6}} \quad (24)$$

the open-loop transfer function in Eq. (23) can be reduced to

$$A_{OL}(s) = \frac{A_0}{\left(1 + \frac{s}{\omega_{dp}}\right)\left(1 + \frac{s}{\omega_{np}}\right)} \quad (25)$$

where the expression for the DC gain A_0 , the dominant pole frequency and the non-dominant pole frequency are given by

$$A_0 = g_{m1}g_{m6}R_xR_y \quad (26)$$

$$\omega_{dp} = \frac{1}{g_{m6}R_xR_yC_C} \quad (27)$$

and

$$\omega_{np} = \frac{g_{m6}C_C}{C_L C_{gs6}} \quad (28)$$

respectively. In the frequencies well above the dominant pole, the open-loop transfer function in (25) can be approximated as

$$A_{OL}(s) = \frac{\omega_{GBW}}{s} \times \frac{1}{1 + \frac{s}{\omega_{np}}} \quad (29)$$

where

$$\omega_{GBW} = A_0 \times \omega_{dp} = \frac{g_{m1}}{C_C} \quad (30)$$

is known as the gain-bandwidth product of the op amp.

Fig. 6 depicts the small-signal equivalent of the op amp in Fig. 4 when connected as an inverting amplifier (Fig. 2(b)). By analyzing the circuit in Fig. 6, under the condition in Eq. (24), the transfer function of the circuit was found to be

$$\frac{v_o(s)}{v_i(s)} = \frac{sC_{gs6} - g_{m6}g_{m1}R_2}{s^2 C_L C_{gs6}(R_1 + R_2) + [g_{m6}C_C(R_1 + R_2) + C_{gs6}]s + g_{m6}g_{m1}R_1} \quad (31)$$

The closed-loop transfer function in Eq. (31) can be re-arranged as

$$A_{CL}(s) = \frac{\left(1 - \frac{s}{z}\right)\omega_o^2}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2} \left(\frac{-R_2}{R_1}\right) \quad (32)$$

where the expression for the zero z , the natural frequency ω_o and the quality factor Q of the closed-loop transfer function are given by

$$z = \frac{g_{m6}g_{m1}R_2}{C_{gs6}} \quad (33)$$

$$\omega_o = \sqrt{\frac{g_{m1}g_{m6}}{\left(1 + \frac{R_2}{R_1}\right)C_L C_{gs6}}} \quad (34)$$

and

$$Q = \frac{\omega_o}{\frac{1}{(R_1 + R_2)C_L} + \frac{g_{m6}C_C}{C_{gs6}C_L}} \quad (35)$$

respectively.

By combining (28) and (35) and setting $Q = 1/\sqrt{2}$, which makes natural frequency to be equal to -3dB bandwidth, i.e., $\omega_o = \omega_{-3\text{dB}}$, we have

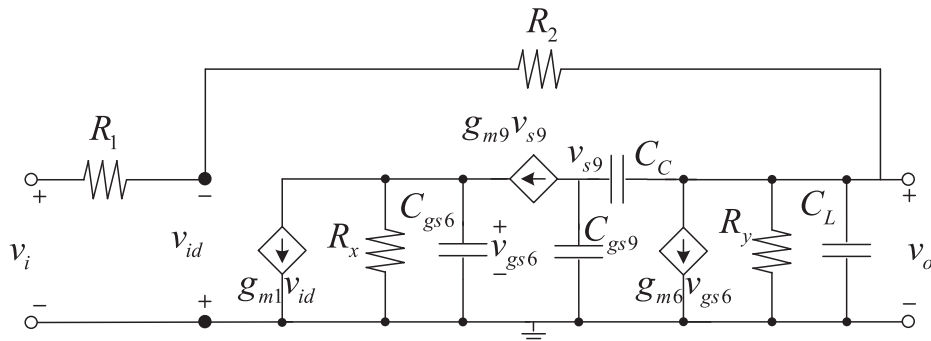


Fig. 6. Small signal of the op amp in Fig. 4 when connected as an inverting amplifier.

$$\omega_{np} = \sqrt{2}\omega_{-3dB} - \frac{1}{(R_1 + R_2)C_L} \quad (36)$$

Also combining (28), (30) and (34) yields

$$g_{m1} = \frac{\omega_{-3dB}^2 C_C \left(1 + \frac{R_2}{R_1}\right)}{\omega_{np}} \quad (37)$$

Substituting (28) into (36) and re-arranging the result, we obtain

$$\omega_{T6} = \frac{g_{m6}}{C_{gs6}} = \left(\sqrt{2}\omega_{-3dB} - \frac{1}{(R_1 + R_2)C_L}\right) \frac{C_L}{C_C} \quad (38)$$

where ω_{T6} is transition frequency of M_6 . Eqs. (37) and (38) can be used to determine the aspect ratios of M_1 and M_6 respectively.

The bias currents I_{D5} and I_{D7} are dictated by slew rate, i.e. $I_{D5} = SR/C_C$ and $I_{D7} = SR(C_C + C_L)/C_C$ and these values are the same for both traditional and the proposed design. However, the value of g_{m9} for the traditional design is given by [17]

$$g_{m9} = \tan\phi_M \omega_u C_L \quad (39)$$

For example, for $\phi_M = 65$ degrees, if the inverting amplifier is designed using approximation equations for closed-loop gain, $A_{o(CL)} \approx 1 - 1/B$, and closed-loop bandwidth, $\omega_{-3dB} \approx B\omega_{ub}$, where B is the feedback factor in Eq. (13), it can be shown that

$$g_{m9} \cong 2.14(1 + |A_{o(CL)}|)\omega_{-3dB}C_L \quad (40)$$

where $A_{o(CL)}$ and ω_{-3dB} are closed-loop DC gain and closed-loop bandwidth of the amplifier respectively. On the other hand, from (24) and (38) the values of g_{m9} for the proposed design can be approximated as

$$g_{m9} \cong \sqrt{2}\omega_{-3dB}C_L - \frac{1}{R_1 + R_2} \quad (41)$$

It can be observed that g_{m9} for the proposed design is somewhat less than g_{m9} for the traditional design, especially when the closed-loop DC gain is greater than unity. As a result, the proposed design would require less current consumption than the traditional design.

4. Simulation results

Based on the two-stage CMOS op amp structure in Fig. 4, comparison will be made between the feedback amplifiers obtained from the proposed design method and the traditional method in which the open-loop op amp is first designed to have 65 degrees phase margin and subsequently employed in the feedback amplifier configuration.

For the process parameters of the AMS 0.35- μm CMOS technology in Table 2 and based on the CMOS op amp in Fig. 4, two inverting amplifiers with DC gain of -2 and bandwidth of 10 MHz, are designed (Fig. 7). The first inverting amplifier is based on traditional design with op amp's open-loop phase margin of 65 degrees. Design parameters of the op amp employed in the first inverting amplifier are obtained from the method in [17]. The second inverting amplifier is based on the proposed design in Section 3, in which the aspect ratios of M_1 , M_6 and M_9 are chosen such that Eqs. (37), (38) and (41) are satisfied. Design parameters of both amplifiers are shown in Table 3. Simulation results of both amplifiers are illustrated in Figs. 8 and 9 and Table 4 respectively. Referring to Figs. 8 and 9, the small-signal AC and transient responses of both inverting amplifiers are comparable. However from Table 4, it can

Table 2
Process parameters.

| Parameters | NMOS | PMOS |
|--------------------------------|------------------------|------------------------|
| $\mu(\text{m/V}\cdot\text{S})$ | 25×10^{-3} | 9.213×10^{-3} |
| $T_{ox}(\text{m})$ | 7.575×10^{-9} | 7.575×10^{-9} |
| $V_t(\text{V})$ | 0.4979 | 0.6842 |

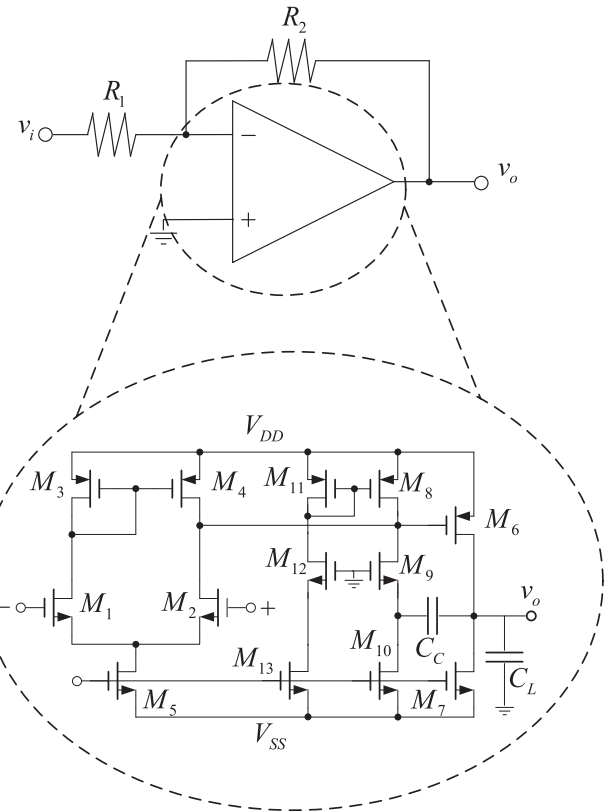


Fig. 7. Inverting amplifier employing two-stage CMOS op amp in Fig. 4.

Table 3
Design parameters.

| Parameters | Traditional ($\phi_M \cong 65^\circ$) | This Work | Unit |
|-----------------|---|-----------|---------------------------|
| $(W/L)_{1,2}$ | 40/1 | 40/1 | $\mu\text{m}/\mu\text{m}$ |
| $(W/L)_{3,4}$ | 11.7/1 | 11.7/1 | $\mu\text{m}/\mu\text{m}$ |
| $(W/L)_5$ | 4.25/5 | 4.25/5 | $\mu\text{m}/\mu\text{m}$ |
| $(W/L)_6$ | 100/3 | 110/5.6 | $\mu\text{m}/\mu\text{m}$ |
| $(W/L)_7$ | 3.4/2 | 3.4/2 | $\mu\text{m}/\mu\text{m}$ |
| $(W/L)_{9,12}$ | 80/0.5 | 15/0.5 | $\mu\text{m}/\mu\text{m}$ |
| $(W/L)_{10,13}$ | 4.95/5 | 2.5/5 | $\mu\text{m}/\mu\text{m}$ |
| $(W/L)_{8,11}$ | 10/1 | 10/1 | $\mu\text{m}/\mu\text{m}$ |
| I_B | 26 | 24 | μA |
| C_C | | 2 | pF |
| C_L | | 2 | pF |
| R_1 | | 100 | k Ω |
| R_2 | | 200 | k Ω |
| Supply Voltage | | ± 2.5 | V |

be observed that the proposed design resulted in the feedback amplifier which consumes significantly less energy than the feedback amplifier obtained from the traditional design.

5. Conclusion

A new method to design feedback amplifier employing two-stage CMOS op amp has been presented. Simulation results confirm that the amplifier obtained from the proposed method consume less power than the amplifier obtained from traditional design (in which op amp's open-loop phase margin is designed to be 65 degrees) by 34% while exhibiting comparable gain, bandwidth, and noise performances.

Declaration of Competing Interest

The authors declare that they have no known competing financial

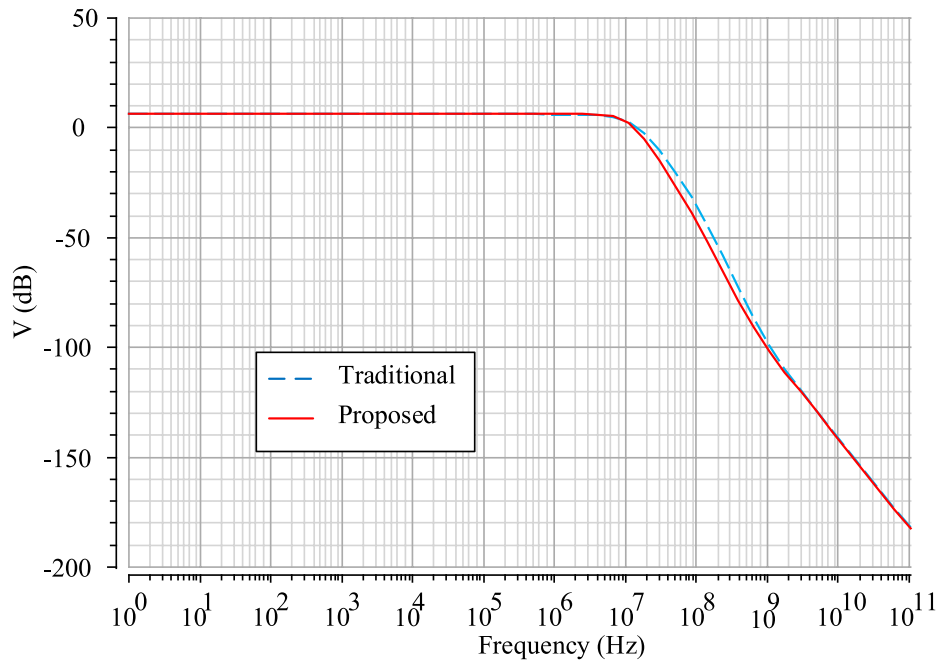


Fig. 8. Frequency response of the simulated inverting amplifiers.

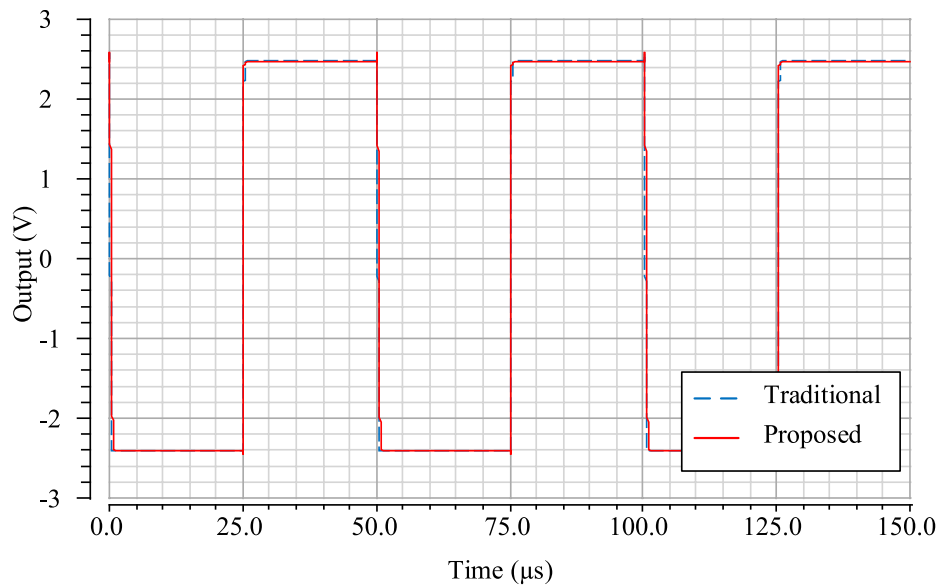


Fig. 9. Transient response of the simulated inverting amplifiers in which the square pulse with amplitude 5 V_{pp} at frequency 20 kHz are applied at the input.

Table 4
Simulation results of inverting amplifiers.

| Parameters | Traditional ($\phi_M \cong 65^\circ$) | Proposed |
|--|---|----------|
| DC gain | 1.99881 | 1.99902 |
| f_{-3dB} (MHz) | 9.8 | 9.9 |
| SR (V/ μ s) | 9.8 | 9.0 |
| Power dissipation (μ W) | 811 | 604 |
| Output noise (μ V _{RMS})(1 Hz-10 MHz) | 318 | 329 |
| $FOM = \frac{f_{-3dB} C_L (pFMHz)}{I_{sup} \mu A}$ | 0.121 | 0.164 |

interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgement

A preliminary version of this work has been published in the 17th international conferences on electrical engineering/ electronics, computer, telecommunications and information technology (ECTI-CON 2020) [23].

References

[1] Trifonov DT, Doorenbos JL. Integrating/SAR ADC and method with low integrator swing and low complexity. U.S. Patent 2008/0258959 A1, October 23, 2008.
 [2] Vural RA, Yildirim T. Analog circuit sizing vis swarm intelligence. Int J Electron Commun (AEU) 2012;66:732-40.

- [3] Teo SA, Tse L, Song Y. Voltage regulator for high performance RF systems. U.S. Patent 8 639 201 B1, January 28, 2014.
- [4] Lo TY, Lo CH. 1-V 365- μ W 2.5-MHz channel selection filter for 3G wireless receiver in 55-nm CMOS. *IEEE Trans Very Large Integ (VLSI) Syst* 2014;22(5):1164–9.
- [5] S RK, Mitikiri Y, Krishanapura N. A 12.5 mW, 11.1nV/-115dB THD, <1 μ s settling, 18-bit SAR ADC driver in 0.6 μ m CMOS. *IEEE Trans Circ Syst* 2015:1–5.
- [6] Mitani Y, Matsukawa K, Obata K, Doshio S. Delta sigma modulator, as well as receiver device and wireless communication device provided. U.S. Patent 9 178 530 B2, November 3, 2015.
- [7] Kumar RSA, Behera D, Krishnapura N. Reset-free memoryless delta-sigma analog-to-digital conversion. *IEEE Trans Circ Syst* 2018:1–11.
- [8] Nasserian M, Peiravi A, Moradi F. A fully-integrated 16-channel EEG readout front-end for neural recording applications. *Int J Electron Commun (AEU)* 2018; 94:109–21.
- [9] Kaya T, Guler H. A hybrid genetic algorithm for active filter component selection. *Int J Electron Commun (AEU)* 2018;86:1–7.
- [10] Rezapour A, Tavakoli MB, Setoudeh F. A new approach for 10-bit pipeline analog-to-digital converter design based on 0.18 μ m CMOS technology. *Int J Electron Commun (AEU)* 2019;99:299–314.
- [11] Kountchou M, Signing VRF, Mogue RLT, Kengne J, Louodop P, Saidou. Complex dynamic behaviors in a new colpitts oscillator topology based on a voltage comparator. *Int J Electron Commun (AEU)* 2020;116:1–17.
- [12] Ahuja BK. An improved frequency compensation technique for CMOS operational amplifiers. *IEEE J Solid-State Circ* 1983;SC-18(6):629–33.
- [13] Johns DA, Martin K. *Analog Integrated Circuit Design*. New York: Wiley; 1997.
- [14] Palmisano G, Palumbo G. A compensation strategy for two-stage CMOS opamp based on current buffer. *IEEE Trans Circ Syst* 1997;44(3):257–62.
- [15] Razavi B. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill Companies; 2000.
- [16] Mahattanakul J, Chutichatuporn J. Design procedure for two-stage CMOS opamp with flexible noise-power balancing scheme. *IEEE Trans Circ Syst* 2005;52(5): 1508–14.
- [17] Mahattanakul J. Design procedure for two-stage CMOS operational amplifiers employing current buffer. *IEEE Trans Circ Syst* 2005;52(11):766–9.
- [18] Sani MT, Hamoui AA. A 1-V process-insensitive current-scalable two-stage opamp with enhanced DC gain and settling behavior in 65-nm digital CMOS. *IEEE J Solid-State Circ* 2011;46(3):660–8.
- [19] Dadashi A, Sadrafahari S, Hadidi K, Khoei A. Fast-settling CMOS op-amp with improved DC-gain. *Analog integr Sig Process* 2012;2012:283–92.
- [20] Vajpayee P. An ultra-high gain low power two stage CMOS op-amp based on inverse aspect ratio self cascode structures. *Analog integr Circ Sig Process* 2014; 2014:349–59.
- [21] De BP, Maji KB, Kar R, Mandal D, Ghoshal SP. Evolutionary computation based sizing technique of nulling resistor compensation based CMOS two-stage op-amp circuit. *Int J High Speed Electron Syst* 2017;26(4):1740021-1–1740021-16.
- [22] Ghosh S, De BP, Kar R, Mal SK. Symbiotic organisms search algorithm for optimal design of CMOS two-stage op-amp with nulling resistor and robust bias circuit. *IET Circ, Dev Syst* 2019;13(5):679–88.
- [23] Chanapromma C, Mahattanakul J. Improved design procedure for two-stage CMOS op amp employing current buffer. *The 17th International Conferences on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON 2020)*, 2020, p. 384–7.
- [24] Gray PR, Hurst PJ, Lewis SH, Meyer RG. *Analysis and Design of Analog Integrated Circuits*. 4th ed. John Wiley & Sons Inc; 2001.
- [25] Allen PE, Holberg DR. *CMOS Analog Circuit Design*. 2nd ed. New York: Oxford University Press; 2002.